

DATA GENERATORS & DATA ANALYZERS

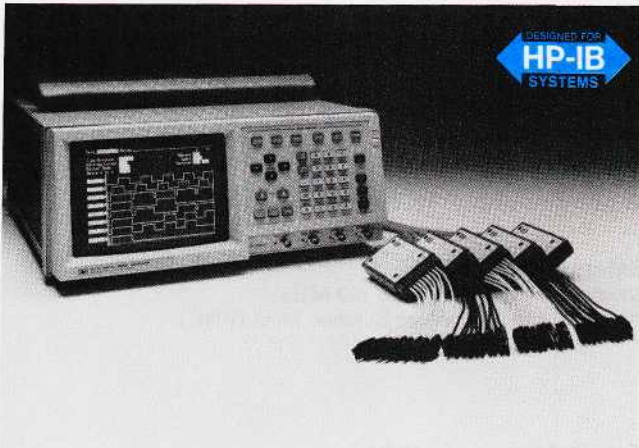
50 MHz Digital/Analog Signal Generator

311

Model 8175A

- 24 channels / 1 kbits ea / 50 Mbits/s ea
2 channels / 8 kbits ea / 100 Mbits/s ea
- Individual pattern duration 20 ns to 9.99 s

- Virtual Memory Expansion
- Interaction with DUT
- Dual Arbitrary Waveform Generator (opt)



HP 8175A with output pods (15461A/15462A/15464A) and trigger pod (15463A)

HP 8175A Digital/Analog Signal Generator

The HP 8175A delivers high-speed parallel and serial data with programmable patterns, adequate for at-speed testing of most of present and future logic circuits. Individually Programmable Pattern Durations permit complex timing set-ups for simulation of extreme, asynchronous timings without wasting memory. Virtual Memory Expansion allows very long data sequences by branching to up to 255 user-definable memory segments. Interaction with a device under test provides for simulation of a wide range of data paths in digital systems. Output pods provide the appropriate levels for most logic families and flexible interface adapters ensure the specified signal quality at the probe tip, a precondition for reliable results.

A Fine Timing option (opt. 001) enhances the timing resolution provided with Programmable Pattern Durations in order to delay four channels with 100 ps.

Operational convenience is stressed through a large, menu driven CRT, a comprehensive data editor including waveform graphics and the capability to directly access (via HP-IB) a printer for documentation and a flexible disc drive for use as a test data library.

In Engineering Test, this versatile feature set provides early simulation of elements not yet available, speeding design cycles through reduced integration time at circuit, module and system level.

In Production Test and Incoming Inspection, automated at-speed testing at the module and system level results in early failure detection, thus reducing production cost and improving quality.

Combining the HP 8175A Digital Signal Generator with a HP 1630/31 family logic analyzer results in a complete Stimulus-Response measurement system. For more information on the HP 1630/31 family logic analyzers refer to the respective pages in this catalog.

Option 002 (Dual Arbitrary Waveform Generator)

With Option 002, the HP 8175A provides two arbitrary channels in addition to the full capabilities of the standard digital signal generator. Thus, some of the stimulation challenges -whether digital, analog or both together- can be met with a single unit (for further information about the analog capabilities, see page 406).

| Address | Location Name | POD | Used | Format | Allocation | Duration |
|---------|---------------|-----|----------|--------|------------|----------|
| 1022 | | 000 | 00000000 | 00 | | 0.02 μs |
| 1023 | | 000 | 00000000 | 00 | | 0.02 μs |
| 0000 | START | 007 | 00000011 | 00 | | 0.05 μs |
| 0001 | | 200 | 00000000 | 00 | | 0.10 μs |
| 0002 | | 000 | 00000011 | 00 | | 0.10 μs |
| 0003 | | 200 | 00000011 | 10 | | 0.25 μs |
| 0004 | | 007 | 00000011 | 11 | | 0.25 μs |
| 0005 | DOWN | 007 | 00000011 | 01 | | 0.15 μs |
| 0006 | | 007 | 00000011 | 01 | | 0.10 μs |
| 0007 | | 207 | 00000011 | 00 | | 0.05 μs |
| 0008 | | 000 | 00000000 | 00 | | 0.10 μs |
| 0009 | | 000 | 00000010 | 00 | | 0.10 μs |
| 0010 | | 000 | 00000010 | 10 | | 0.25 μs |
| 0011 | UP | 002 | 00000010 | 11 | | 0.25 μs |
| 0012 | | 002 | 00000010 | 01 | | 0.15 μs |
| 0013 | | 002 | 00000010 | 01 | | 0.10 μs |

Data Page: Pattern Set-Up

Data can be entered and displayed in various codings. Channels to be displayed can be selected. Comprehensive data editing support is provided. For instance, segments can be moved or copied to other memory addresses or data segments can be 'block modified'. Easy exchange of data between channels avoids having to rearrange probes at the test fixture. Also, fixed patterns such as up and down counters with selectable start and stop address are loaded with a few key-strokes. All codings from the pattern Set-Up page will be automatically converted into a timing diagram when switched to this page. Or, the data can be set-up from scratch or easily edited in terms of waveforms.

| Step | Segment Name | Label or Address | Label or Address | Repetition Times |
|------|--------------|------------------|------------------|------------------|
| 000 | INIT | from 000 | to 100 | 001 |
| 001 | CLEAR | from 21 | to 120 | 014 |
| 015 | TEST1 | from 200 | to UP | 002 |
| 017 | | from 250 | to 270 | 001 |
| | | end | | |
| 018 | TEST2 | from 991 | to 120 | 001 |
| 019 | | from 300 | to 300 | 001 |
| | | end | | |

Program Page: Segment Assignment

This page gives an example of how pattern sequencing can be defined. Up to 255 segments of data memory can be defined by first and last addresses or labels in the 0000 to 1023 address range. During data execution the segments are real-time sequenced in the given order thus virtually expanding the memory depth far beyond the physical depth of 1024 data patterns.

DATA GENERATORS & DATA ANALYZERS

50 MHz Digital/Analog Signal Generator (cont'd)

Model 8175A

Specifications

Specifications apply for operating temperatures from 0°C to 55°C.

Parallel / Serial Data Generator

Number of channels: 24 parallel, 2 serial

Bits per channel: 1024 parallel, 8192 serial

Max. NRZ Bit rate per ch.: 50 Mbit/s parallel, 100 Mbit/s serial

Pattern Duration (with internal clock):

In *Parallel* mode the duration of each individual pattern is programmable. In *Serial* mode the duration of the data bits is programmable with successive bits always having the same duration. The duration is equal for all channels.

| | | |
|-------------------|-----------------------------|--------------|
| Range/Resolution: | (10)*, 20 ns - 9.99 μ s | /10 ns |
| | 10 μ s - 999 MS | /1 MS |
| | 1 ms - 99.9 ms | /100 μ s |
| | 0.1 s - 9.99 s | /10 ms |

*10 ns in serial mode with fixed timing

Accuracy: $\pm 0.05\%$ of progr. duration ± 2.5 ns
(asynchronous start)
 $\pm 0.5\%$ of progr. duration ± 2.5 ns
(synchr. start, clock calibration)
 $\pm 3.0\%$ of progr. duration ± 2.5 ns
(synchr. start, no clock cal.)

Jitter (max.): 0.1% of progr. value +150ps

Pattern Duration (with external clock):

| | | |
|--------------------------|----------------|---------------------|
| Period of ext. clock x m | (Range) | / Resolution: |
| (1)2** | to 999 | / 1 period |
| 1 000 | to 99 900 | / 100 periods |
| 100 000 | to 9 990 000 | / 10 000 periods |
| 10 000 000 | to 999 000 000 | / 1 000 000 periods |

*Min. Pattern duration in parallel mode 20ns, in serial mode 10ns.

Clock

The clock has a programmable period. It is available on line 7 of the pod for the output flags. In serial mode an additional Clock is available providing a pulse at every bit.

Period (with internal clock):

Range / Resolution: 20ns - 9.99MS / 10ns; 2MS - 999MS / 1 μ s

Accuracy: $\pm 0.05\%$ of progr. value $\pm 2.5\mu$ s
(asynchronous start)
 $\pm 0.5\%$ of progr. value $\pm 2.5\mu$ s
(synchr. start, clock cal.)
 $\pm 3\%$ of progr. value $\pm 2.5\mu$ s
(synchr. start, no clock cal.)

Period (with external clock):

Period of external clock x m

Range: m = 2,3,4 . . . 999, 1000, 1100, 1200, . . . 99 900

Skew (maximum time difference between the leading or trailing data bit edges of the same memory address with Fine Timing off)

across ECL pods: <6 ns; typical <3 ns

across TTL/CMOS pods: <7 ns; typical <3 ns

Option 001 Fine Timing

(can be retrofitted in HP service office)

Parallel Data Generator

Channels: 0,1,2 and 3 of pod 0

Delay (Range/Resolution): 20 ns to 40 ns / 100 ps

Accuracy: $\pm 5\%$ of progr. value ± 1 ns

Serial Data Generator

Channels: 0 and 2 of pod 0

Delay (Range/Resolution): 0 ns to 20 ns / 100 ps

Accuracy: $\pm 5\%$ of progr. value ± 2 ns

External Input (BNC)

This connector can be used to start / stop datacycling with selectable transitions.

Impedance: 10kohm/50 pF

Threshold (Range/Resolution): -9.9V to +9.9 V/100 mV

Accuracy: $\pm 5\%$ of progr. value ± 250 mV

Min. swing: 600 mV pp

Min. overdrive: 250 mV or 30% of input amplitude

Max. input voltage: ± 20 V

External Clock (BNC)

Clock rate (Range): 8Hz to 100 MHz

All other specifications see External Input (BNC).

External Reference (BNC)

Input characteristics: LS TTL compatible

Ordering Information

HP 8175A Digital/Analog Signal Generator

Note: HP 8175A must be ordered with at least one of the options #002, #003, #004, #005 or individual pods, as required.

Options:

Opt. 001 Fine Timing; 4 channels, 100 ps resolution

Opt. 002 Dual Arbitrary Waveform Generator

Opt. 003 Set of 4 ECL Pods Model HP 15461A and 1 Trigger Pod Model HP 15463A

Opt. 004 Set of 4 TTL Pods Model HP 15464A and 1 Trigger Pod Model HP 15463A

Opt. 005 Set of 4 TTL/CMOS Pods Model HP 15462A and 1 Trigger Pod Model HP 15463A

Opt. 908 Rack Flange Kit (PN 5061-9678)

Opt. 910 Additional Operating/Programming/Service Manual

Opt. 916 Additional Operating/Programming Manual

Pods:

HP 15461A ECL Pod (fixed ECL levels, includes 1 ea HP 15429A)

HP 15462A TTL/CMOS Pod (programmable High Level, incl. 1 ea HP 15429A)

HP 15463A Trigger Pod (includes lead set and 10 ea probe tip)

HP 15464A TTL Pod (fixed TTL levels, includes 1 ea HP 15429A)

Adaptors for HP 15461A, HP 15462A and HP 15464A:

HP 15408A plug-on grabbers with ground leads 5 ea

HP 15409A plug-on BNC adaptors, 5 ea

HP 15410A plug-on SMB adaptors, 5 ea

HP 15411A plug-on coax open-end adaptors, 5 ea

HP 15415A plug-on miniprobe, usable with HP 10024A IC clip, 5 ea

HP 15429A solder-in receptacles (standard accessory, 5x2 ea)

Adaptors for HP 15463A:

HP PN 15463-63201 lead set

HP PN 10230-62101 probe tip, 1 ea (10 ea necessary per pod)

Others:

HP 15430A cable for synchronized master-slave operation of two ea HP 8175A

HP 10062A Protective Cover (for front panel)